REMARKS

The Applicants note that the Office Action Summary does not indicate whether the drawings filed in the application are acceptable. Confirmation of their acceptability is respectfully requested.

It is noted that claims 5-6, 13, 17, 21, 24 and 29 are objected to but would be allowable if rewritten in independent form.

Claims 1-4, 7-8, 14-16, 22-23 and 25-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohmuro, *et al.* (U.S. Publication Number 2006/0017677) in view of Maeda, *et al.* (U.S. Patent Number 6,091,389). Claims 9-12 and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohmuro, *et al.* in view of Younis, *et al.* (U.S. Patent Number 6,292,122). In view of the following remarks, the rejections are respectfully traversed, and reconsideration of the rejections is requested.

In the present invention as claimed in claims 1-13 and 22-25, a response time accelerator for driving a liquid crystal display (LCD) includes a frame memory unit that updates and stores one or more frames of previous data and an acceleration unit that reads the previous data corresponding to input current data and performs interpolations on a decoded mapped panel output value and mapped panel characteristic value according to flag information, and the acceleration unit generates liquid crystal panel data to be output to a liquid crystal panel and previous data of a next frame to be output to the frame memory unit. The acceleration unit determines a gray level at which to generate the liquid crystal panel data based on the flag information set in a previous frame. The flag information for a next frame is set based on a comparison of the current data and the previous data of a next frame.

In the present invention as claimed in claims 14-21 and 26, a method for improving a response time of a liquid crystal panel performed in a response time accelerator having a frame memory unit for updating and storing one or more frames of previous data and an acceleration unit includes performing interpolation on a decoded predetermined mapped panel output value according to flag information and generating liquid crystal panel data to be output to the liquid crystal panel in the acceleration unit. The method further includes reading the previous data corresponding to the current data

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in the acceleration unit, performing interpolation on a decoded predetermined mapped panel characteristic value according to the flag information and generating liquid crystal panel data to be output to the liquid crystal panel in the acceleration unit, and performing interpolation on the decoded predetermined mapped panel characteristic value according to the flag information and generating previous data of a next frame to be output to the frame memory unit in the acceleration unit. A gray level at which to generate the liquid crystal panel data is determined based on the flag information set in a previous frame, and the flag information for a next frame is set based on a comparison of the current data and the previous data of a next frame.

In the present invention as claimed in claims 27-29, an acceleration unit performs interpolation on current data based on flag information set in a previous frame and generates flag information for a next frame based on a comparison of the current data and the previous data of a next frame.

Ohmuro, *et al.* discloses that a drive control part 50 outputs a target drive signal S12 in correspondence with the transmittance of the pixels and is alternately stored in primary and secondary frame memories 53, 54 in each frame period. The Office Action states that item 53, the primary frame memory, is analogous to the claimed frame memory unit. The only signal received by the primary frame memory 53 is the target drive signal from the drive control part 50. A display status change pixel detection circuit 55 outputs a compensation voltage signal S14 to a drive voltage adjustment circuit 57. The drive voltage adjustment circuit 57 adds the compensation voltage signal S14 to the target drive signal S12 supplied from the drive control part 50 and supplies it to a source driver part 59 as the drive signal S13. The Office Action analogizes items 53-58 to the claimed acceleration unit. However, in Ohmuro, *et al.*, the drive signal S13 is provided to the source driver 59 of the liquid crystal display device. Neither of the outputs from items 53-58, i.e., the compensation voltage S14 and the drive signal S13, are supplied to the primary frame memory 53.

As stated in Amendment B dated July 12, 2007, Ohmuro, *et al.* fails to teach or suggest a response time accelerator for driving an LCD that includes an acceleration unit that generates liquid crystal panel data to be output to a liquid crystal panel and previous data of a next frame to be output to the frame memory unit, as claimed in claims 1-13 and 22-25. Instead, in Ohmuro, *et al.*, the only signal received by the primary frame memory

53 is the target drive signal from the drive control part 50 and neither of the outputs from items 53-58, i.e., the compensation voltage S14 and the drive signal S13, are supplied to the primary frame memory 53. Therefore, in Ohmuro, *et al.*, previous data of a next frame are not output from any of the items 53-58 to either of the primary frame memory 53 or the secondary frame memory 54.

Further, as stated, in Amendment B dated July 12, 2007, Ohmuro, *et al.* fails to teach or suggest a method for improving a response time of a liquid crystal panel performed in a response time accelerator having a frame memory unit for updating and storing one or more frames of previous data and an acceleration unit that includes generating liquid crystal panel data to be output to the liquid crystal panel in the acceleration unit and generating previous data of a next frame to be output to the frame memory unit in the acceleration unit, as claimed in claims 14-21 and 26. Instead, in Ohmuro, *et al.*, the only signal received by the primary frame memory 53 is the target drive signal from the drive control part 50 and neither of the outputs from items 53-58, i.e., the compensation voltage S14 and the drive signal S13, are supplied to the primary frame memory 53. Therefore, in Ohmuro, *et al.*, previous data of a next frame are not output from any of the items 53-58 to either of the primary frame memory 53 or the secondary frame memory 54.

With regard to the flag information feature of the invention set forth in the claims, the Office Action states, at page 3, line 20 through page 4, line 2 and page 6, lines 3-6, "Ohmuro, *et al.* does not teach wherein an acceleration unit determines a gray level at which to generate the liquid crystal panel data based on the flag information set in a previous frame, and wherein the flag information for a next frame is set based on a comparison of current data and the previous data of the next frame."

Therefore, Ohmuro, *et al.* fails to teach or suggest a response time accelerator for driving an LCD that includes an acceleration unit that determines a gray level at which to generate the liquid crystal panel data based on flag information set in a previous frame, the flag information for a next frame being set based on a comparison of the current data and the previous data, as claimed in claims 1-13 and 22-25.

In addition, Ohmuro, *et al.* fails to teach or suggest a method for improving a response time of a liquid crystal panel performed in a response time accelerator having a frame memory unit for updating and storing one or more frames of previous data and an

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acceleration unit that includes the acceleration unit determining a gray level at which to generate the liquid crystal panel data based on the flag information set in a previous frame, the flag information for a next frame being set based on a comparison of the current data and the previous data of a next frame, as claimed in claims 14-21 and 26.

In addition, Ohmuro, *et al.* fails to teach or suggest a response time accelerator that includes an acceleration unit that performs interpolation on current data based on flag information set in a previous frame and generates flag information for a next frame based on a comparison of the current data and the previous data of a next frame, as claimed in claims 27-29.

Maeda, *et al.* discloses partially rewriting a display. A change point extraction unit 2550 detects a change point between frames by comparison between an input binarized signal and a binarized signal before one frame stored in frame memory, and compares its sum with a threshold, wherein if the sum is greater than a threshold, that point is extracted as a change point and the flag in the line flag memory 560 corresponding to a scan line of interest is set. Before starting the process of scan lines, corresponding flags in the line flag memory 560 are reset. If no change point exists within one scan line, the flag in the line flag memory 560 for the scan line of interest remains reset. A partial write detection unit 680 monitors the flag status in line flag memory 670, and if any flag is set, the partial write from the corresponding scan line is performed.

Maeda, *et al.* fails to teach or suggest a response time accelerator for driving an LCD that includes an acceleration unit that generates liquid crystal panel data to be output to a liquid crystal panel and previous data of a next frame to be output to the frame memory unit, as claimed in claims 1-13 and 22-25.

Maeda, *et al.* fails to teach or suggest a method for improving a response time of a liquid crystal panel performed in a response time accelerator having a frame memory unit for updating and storing one or more frames of previous data and an acceleration unit that includes generating liquid crystal panel data to be output to the liquid crystal panel in the acceleration unit and generating previous data of a next frame to be output to the frame memory unit in the acceleration unit, as claimed in claims 14-21 and 26.

With regard to the flag information feature of the invention set forth in the claims, Maeda, *et al.* fails to teach or suggest a response time accelerator for driving an LCD that

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includes an acceleration unit that determines a gray level at which to generate the liquid crystal panel data based on flag information set in a previous frame, the flag information for a next frame being set based on a comparison of the current data and the previous data, as claimed in claims 1-13 and 22-25. Instead, in Maeda, *et al.*, before starting the process of scan lines, corresponding flags in the line flag memory 560 are reset. In Maeda, *et al.*, if a change point is detected, the flag in the line flag memory 560 is set, and if no change point exists, the flag in the line flag memory 560 is reset. Therefore, the flag of a previous frame has no affect on the partially rewritten data, because the flags in the line flag memory 560 are reset before each scan process. In addition, there is no teaching or suggestion in Maeda, *et al.* that the flag has any effect on the gray levels at which the partial write data are generated. The flag information of Maeda, *et al.* indicates whether the pixel data is to be rewritten with no regard to the gray level.

In addition, Maeda, *et al.* fails to teach or suggest a method for improving a response time of a liquid crystal panel performed in a response time accelerator having a frame memory unit for updating and storing one or more frames of previous data and an acceleration unit that includes the acceleration unit determining a gray level at which to generate the liquid crystal panel data based on the flag information set in a previous frame, the flag information for a next frame being set based on a comparison of the current data and the previous data of a next frame, as claimed in claims 14-21 and 26. Instead, in Maeda, *et al.*, before starting the process of scan lines, corresponding flags in the line flag memory 560 are reset. In Maeda, *et al.*, if a change point is detected, the flag in the line flag memory 560 is set, and if no change point exists, the flag in the line flag memory 560 is reset. Therefore, the flag of a previous frame has no affect on the partially rewritten data, because the flags in the line flag memory 560 are reset before each scan process. In addition, there is no teaching or suggestion in Maeda, *et al.* that the flag has any affect on the gray levels at which the partial write data are generated. The flag information of Maeda, *et al.* indicates whether the pixel data is to be rewritten with no regard to the gray level.

In addition, Maeda, *et al.* fails to teach or suggest a response time accelerator that includes an acceleration unit that performs interpolation on current data based on flag information set in a previous frame and generates flag information for a next frame based on a comparison of the current data and the previous data of a next frame, as claimed in

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claims 27-29. Instead, in Maeda, *et al.*, before starting the process of scan lines, corresponding flags in the line flag memory 560 are reset. In Maeda, *et al.*, if a change point is detected, the flag in the line flag memory 560 is set, and if no change point exists, the flag in the line flag memory 560 is reset. Therefore, the flag of a previous frame has no effect on the partially rewritten data, because the flags in the line flag memory 560 are reset before each scan process.

Therefore, Ohmuro, *et al.* and Maeda, *et al.* fail to teach or suggests elements of the present invention set forth in claims 1-13, 22-25, 14-21, 26 and 27-29. Specifically, Ohmuro, *et al.* and Maeda, *et al.* fail to teach or suggest a response time accelerator for driving an LCD that includes an acceleration unit that generates liquid crystal panel data to be output to a liquid crystal panel and previous data of a next frame to be output to the frame memory unit and that determines a gray level at which to generate the liquid crystal panel data based on flag information set in a previous frame, the flag information for a next frame being set based on a comparison of the current data and the previous data, as claimed in claims 1-13 and 22-25. In addition, Ohmuro, *et al.* and Maeda, *et al.* fail to teach or suggest a method for improving a response time of a liquid crystal panel performed in a response time accelerator having a frame memory unit for updating and storing one or more frames of previous data and an acceleration unit that includes generating liquid crystal panel data to be output to the liquid crystal panel in the acceleration unit and generating previous data of a next frame to be output to the frame memory unit in the acceleration unit, and the acceleration unit determining a gray level at which to generate the liquid crystal panel data based on the flag information set in a previous frame, the flag information for a next frame being set based on a comparison of the current data and the previous data of a next frame, as claimed in claims 14-21 and 26. In addition, Ohmuro, *et al.* and Maeda, *et al.* fail to teach or suggest a response time accelerator that includes an acceleration unit that performs interpolation on current data based on flag information set in a previous frame and generates flag information for a next frame based on a comparison of the current data and the previous data of a next frame, as claimed in claims 27-29. Since neither reference teaches these claimed elements of the invention, there is no way to combine the references to obtain teaching or suggestion of the claimed elements. The Ohmuro, *et al.* and Maeda, *et al.* references, taken alone or in combination, fail to teach or suggest these elements of the claimed

invention. Therefore, it is believed that the claims are allowable over the cited references, and reconsideration of the rejections of claims 1-4, 7-8, 14-16, 22-23 and 25-28 under 35 U.S.C. § 103(a) based on Ohmuro, *et al.* and Maeda, *et al.*, is respectfully requested.

Younis, *et al.* is cited in the Office Action as teaching predetermined mapped panel output values and predetermined mapped panel characteristics values that correspond one-to-one to gray level values determined by MSB bits of the current data and previous data.

Like Ohmuro, *et al.* and Maeda, *et al.*, Younis, *et al.* fails to teach or suggest a response time accelerator for driving an LCD that includes an acceleration unit that generates liquid crystal panel data to be output to a liquid crystal panel and previous data of a next frame to be output to the frame memory unit, as claimed in claims 1-13 and 22-25. In addition, like Ohmuro, *et al.* and Maeda, *et al.*, Younis, *et al.* also fails to teach or suggest a response time accelerator for driving an LCD that includes an acceleration unit that determines a gray level at which to generate the liquid crystal panel data based on flag information set in a previous frame, the flag information for a next frame being set based on a comparison of the current data and the previous data, as claimed in claims 1-13 and 22-25.
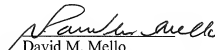
Like Ohmuro, *et al.* and Maeda, *et al.*, Younis, *et al.* further fails to teach or suggest a method for improving a response time of a liquid crystal panel performed in a response time accelerator having a frame memory unit for updating and storing one or more frames of previous data and an acceleration unit that includes generating liquid crystal panel data to be output to the liquid crystal panel in the acceleration unit and generating previous data of a next frame to be output to the frame memory unit in the acceleration unit, as claimed in claims 14-21 and 26. In addition, like Ohmuro, *et al.* and Maeda, *et al.*, Younis, *et al.* also fails to teach or suggest a method for improving a response time of a liquid crystal panel performed in a response time accelerator having a frame memory unit for updating and storing one or more frames of previous data and an acceleration unit that includes the acceleration unit determining a gray level at which to generate the liquid crystal panel data based on the flag information set in a previous frame, the flag information for a next frame being set based on a comparison of the current data and the previous data of a next frame, as claimed in claims 14-21 and 26.

Hence, neither of Ohmuro, *et al.*, as discussed above, and Younis, *et al.* teaches or suggests specific elements of the present invention set forth in claims 1-13, 22-25 and 14-21 and 26. Accordingly, there is no combination of the references which would provide such teaching or suggestion. Neither of the references, taken alone or in combination, teaches or suggests the invention set forth in the amended claims. Therefore, it is believed that the claims are allowable over the cited references, and reconsideration of the rejections of claims 9-12 and 18-20 under 35 U.S.C. § 103(a) based on Ohmuro, *et al.* and Younis, *et al.* is respectfully requested.

In view of the foregoing remarks, it is believed that all claims pending in the application are in condition for allowance, and such allowance is respectfully solicited. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

Date: _Dec. 26, 2007_
Mills & Onello, LLP
Eleven Beacon Street, Suite 605
Boston, MA 02108
Telephone: (617) 994-4900
Facsimile: (617) 742-7774
J:\SAM\0457\amendmentc.doc

David M. Mello
Registration Number 43,799
Attorney for Applicants